

FIG. 2

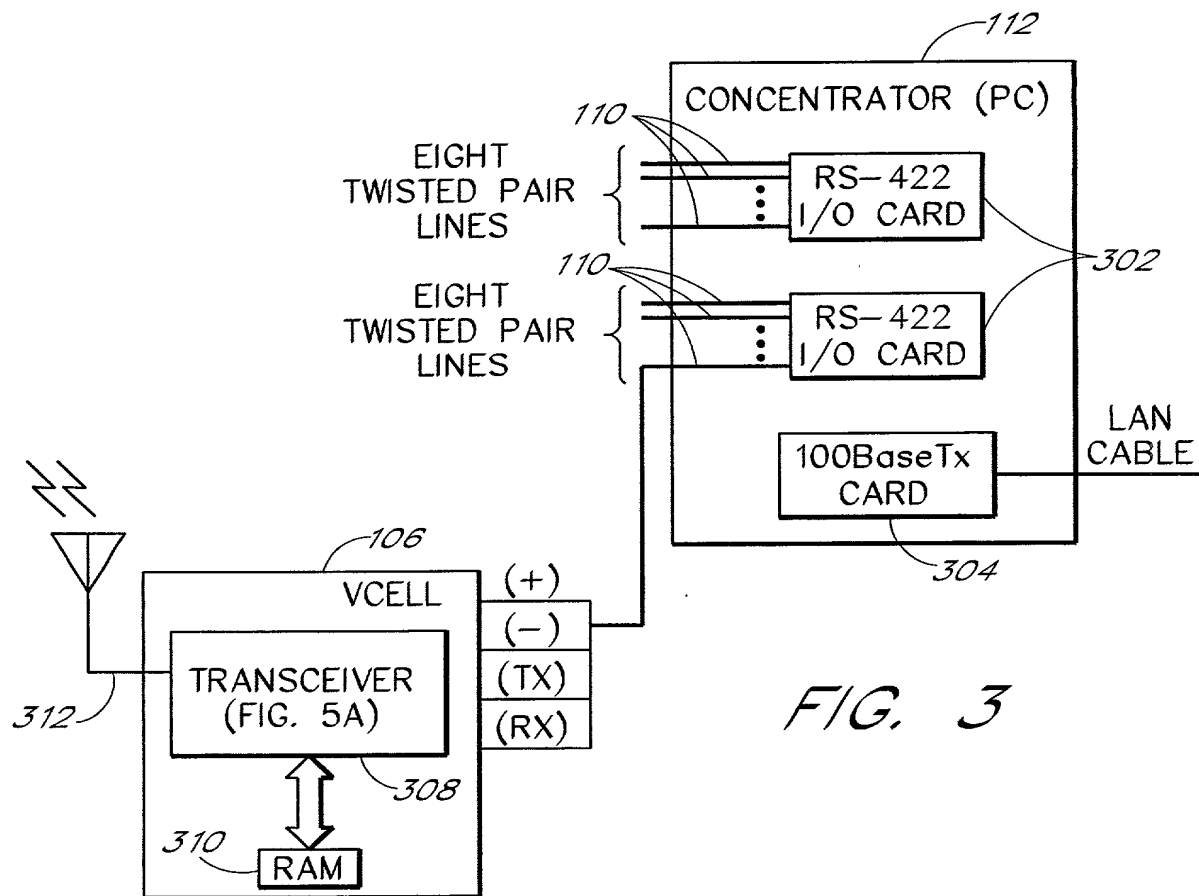


FIG. 3

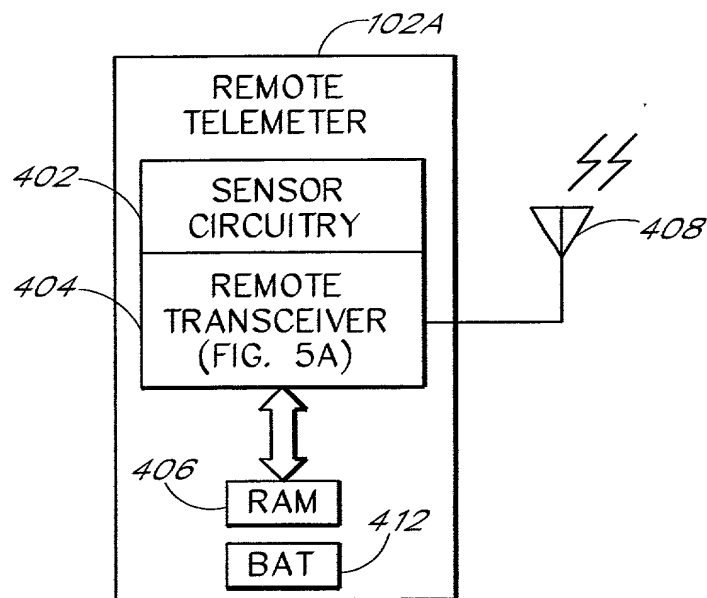


FIG. 4

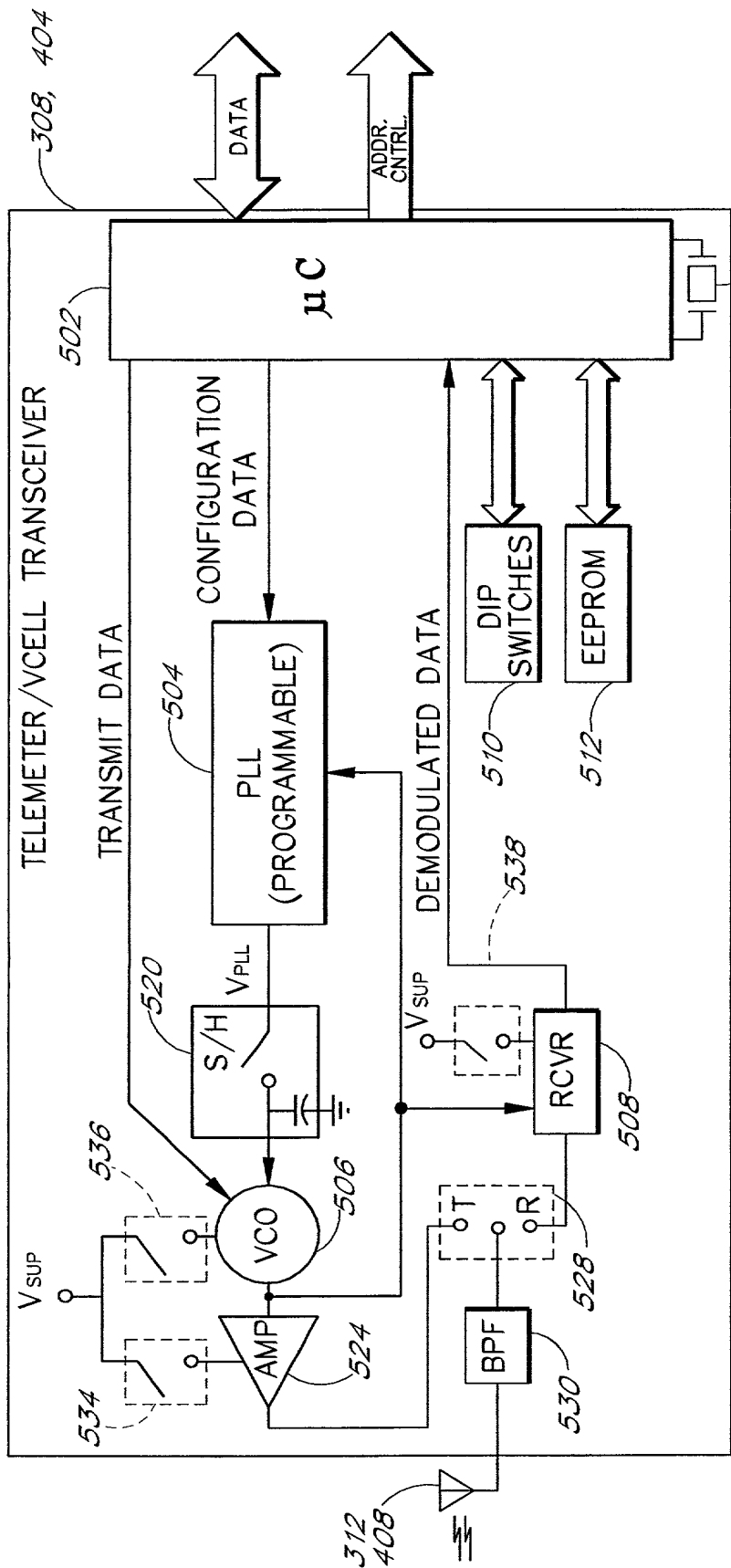


FIG. 5A

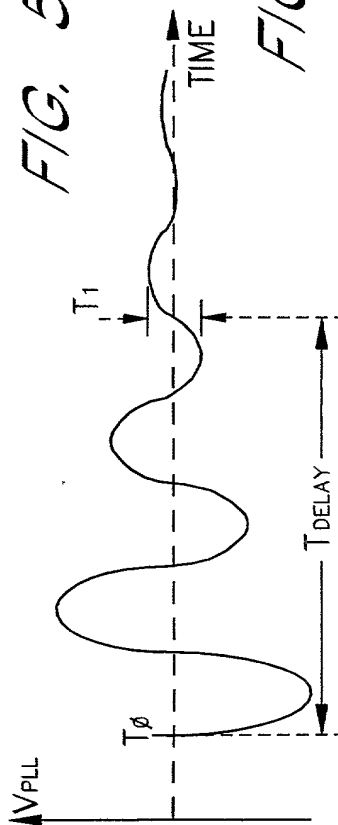


FIG. 5B

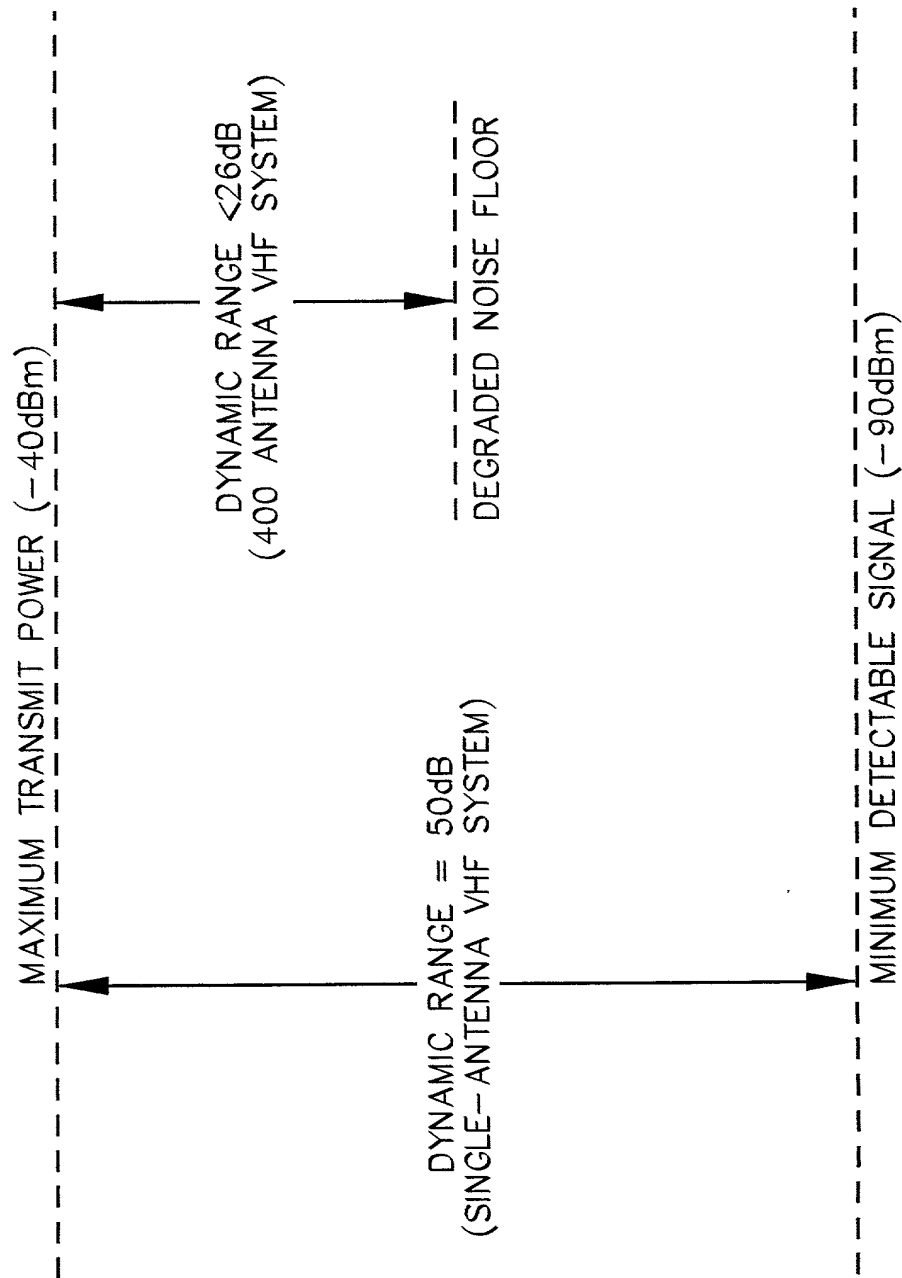


FIG. 6

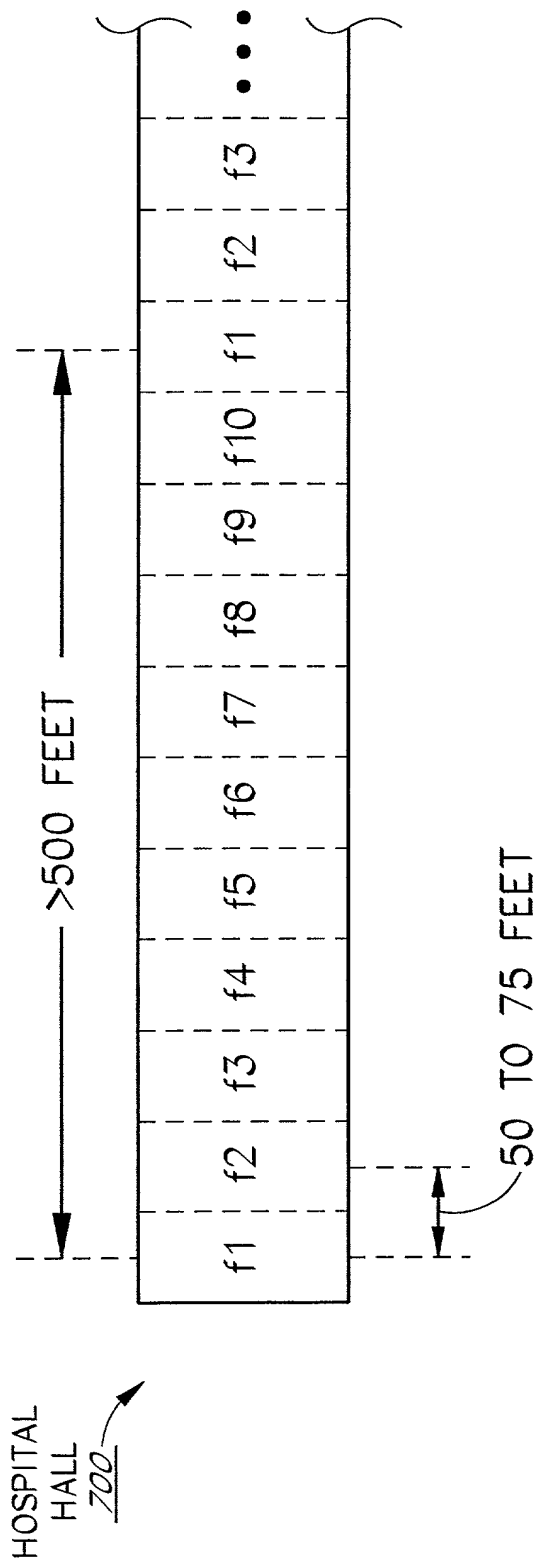


FIG. 7

TIMESLOT STATUS TABLE

900



	SLOT 1	SLOT 2	SLOT 3	SLOT 4	SLOT 5	SLOT 6
ASSIGNED	✓	✓		✓	✓	
FRAMES SINCE LAST PACKET	0	0	(NA)	3	0	(NA)

FIG. 9

VCELL CATALOG

1100



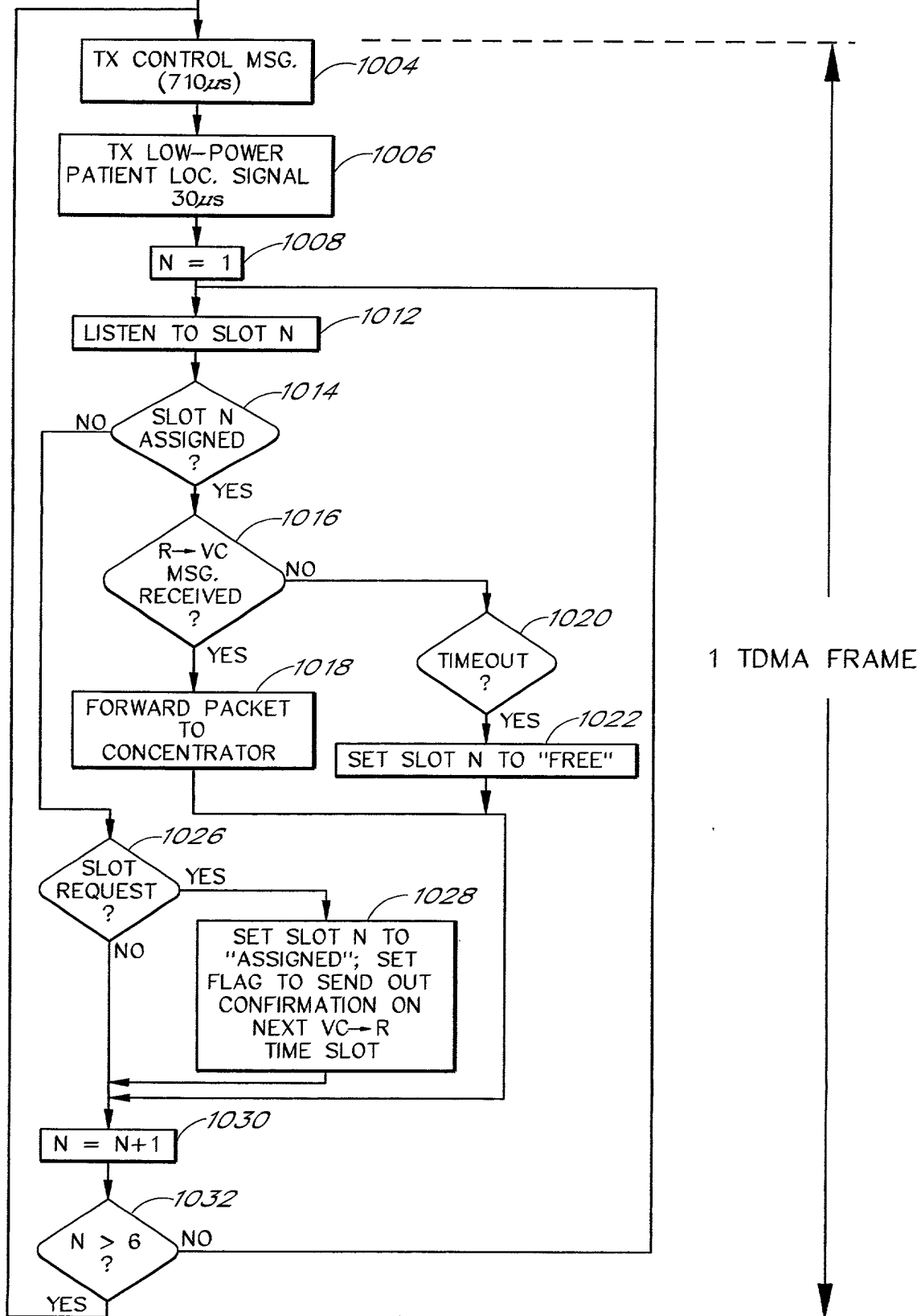
	RATING	CONNECTED TO	LOW-PWR. SIGNAL STRENGTH
VCELL1 (f1)	7		1
VCELL2 (f2)	8	✓	9
VCELL3 (f3)	8		6
VCELL4 (f4)	8	✓	6
VCELL5 (f5)	6		1
VCELL6 (f6)	2		0
VCELL7 (f7)	0		0
VCELL8 (f8)	0		0
VCELL9 (f9)	3		0
VCELL10 (f10)	5		1

FIG. 11

POWER-ON
INITIALIZATION
(SET ALL R→VC
TIMESLOTS TO "FREE")

VCELL PROTOCOL
1000

FIG. 10



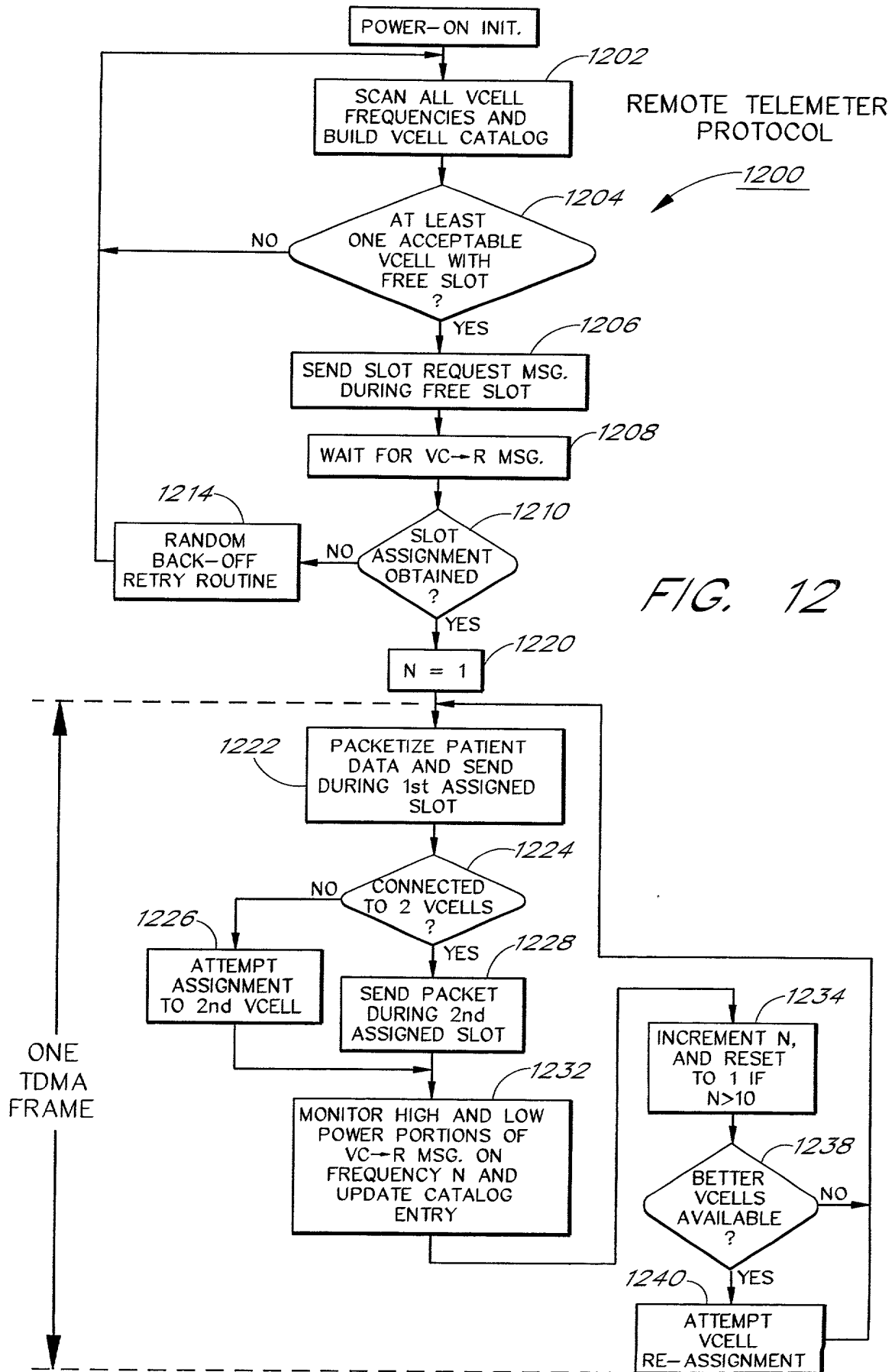


FIG. 12

FIG. 13

